Boost Type Multilevel Delta-Connection Cascaded Inverter

Transformerless, Multilevel inverter, Boost function

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Abstract

In response to the demand for high voltage, large capacity, and low distortion power converters, multilevel inverters are found to be useful. There are some circuit methods where high voltage is output using a multilevel inverter, and representative examples now one include a cell cascaded multilevel method. The cell cascaded multilevel method is a method whereby a single-phase AC inverter cell is connected in series. In general, this method needs an isolated DC voltage source to each cell. Therefore, a multiphase transformer and rectifiers are required. Therefore we developed a cascaded multilevel inverter that was transformer-less in simulation. This cascaded multilevel inverter will offer three unique features as itemized below.

(1) Transformer-less configuration (downsizing)
(2) Reducing distortion of output voltage by control of capacitor voltage
(3) By a boost voltage function, it enables higher output voltage than the input voltage

1. Preface

In the current industrial sector, the demand for technologies to realize larger capacity and higher voltage power converter has increased. In response to such a challenge, cascaded multilevel inverters are currently being researched in industry. At present, the best known multilevel topologies to realize the boost output voltages are three typical methods: the cell cascade inverters, the diode-clamped multilevel inverter, and the flying capacitor multilevel inverter. The cell cascade inverter uses a method to connect single-phase inverter cells to a series. By increasing the number of cascaded inverter cells in series, cascade inverter enables the output voltage to be increased without increasing the breakdown voltage of the switching components.

In addition, the output waveform is several steps shape when the output voltage is made many levels. Because the number of these steps increases, one step of change width of the output voltage becomes small and the output harmonics decrease. On the one hand, however, in general, it requires one isolated DC voltage source for each inverter cell so that a multiphase transformer and rectifiers are required. If a multiphase transformer is used, input currents in different phases are synthesized. As a result, harmonics in source-side currents are decreased, but the number of cables on secondary side is increased, thus increasing the overall mass and size of equipment as a whole. As a result, bulky inverter size becomes an issue.

This paper introduces a new cell cascaded multilevel method. This method does not require any multiphase transformer and it can be operated by one DC voltage source.

2. Conventional Cell Series-Connected Multilevel Inverters

Fig. 1 shows topologies of two different cell cascaded multilevel inverters: one is in a star connection and the other is in a delta connection. Both inverters are constructed with a multiphase transformer and six inverter cells. Each inverter cell is composed of a rectifier and a single-phase full-bridge inverter, and a DC link capacitor connecting them. By these two methods, the number of the levels of the condenser voltage of each inverter cell and the output voltage is different. Compared with the two-level inverters, each different method has the following features:

(1) Because a cell is connected to a series, the DC voltage per unit cell is lowered.
(2) Voltage change width becomes small with the multilevel output voltage, and the reduction of harmonics is bettered.

In general, however, the cascaded multilevel inverter requires one isolated DC voltage source to each cell. This DC voltage source is composed of a multiphase transformer and a diode rectifier. Therefore, by this method, the wiring amount of the multiphase transformer second side increases or otherwise upsizing of the device becomes the problem.

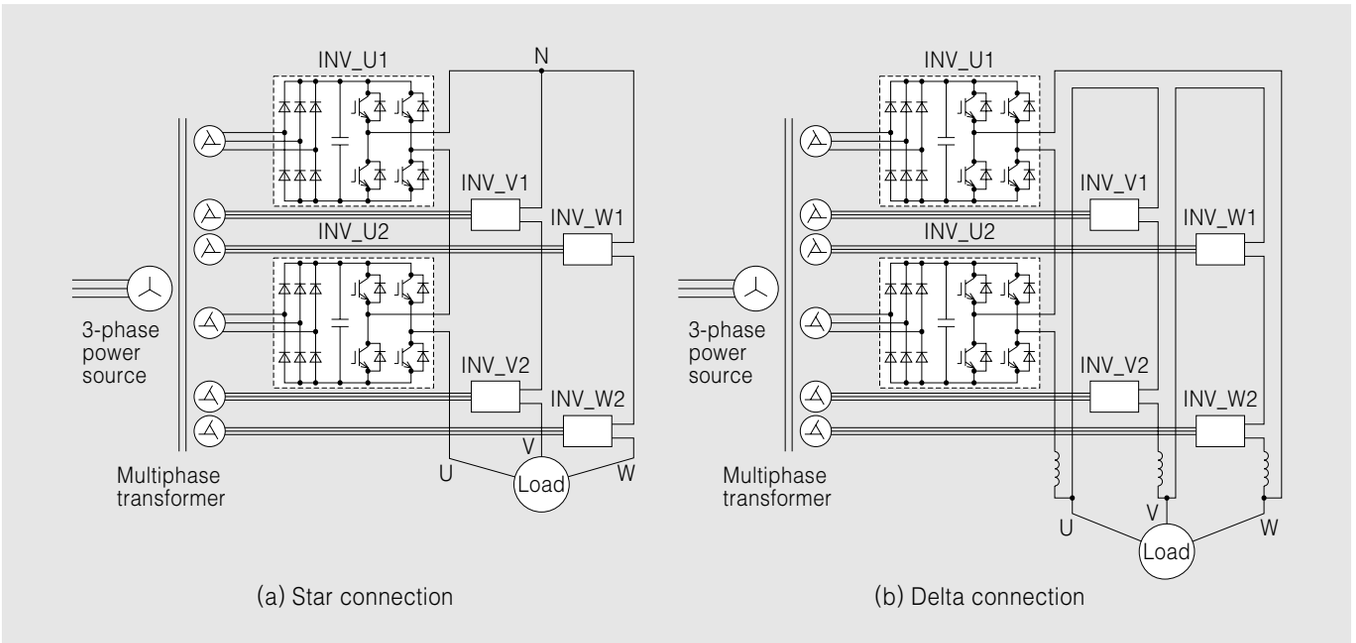

Fig. 1 Multilevel Inverters in Different Connections

Topologies of two type cascade inverters with different connections are shown. Both of these two inverters require one isolated DC voltage source for each cell.

3. Boost Type Multilevel Delta-Connection Cascaded Inverter

The Y connection and the Δ connection of the cell cascaded multilevel method are shown in Fig. 1. We developed a boost type multilevel delta-connection cascaded inverter technology to improve upsizing of the device, which was a problem of the cell cascaded multilevel method.

3.1 Circuit Configuration

Fig. 2 shows a boost type multilevel delta-connection cascaded inverter. This circuit involves a DC single voltage source consisting of diode rectifiers and six inverter cells. One set of two inverter cells is allocated between P and N of V_{DC}, and outputs are arranged in delta-connection. Each inverter cell has a boost converter and an inverter connected by a small DC link capacitor C_{DC}. Since each inverter cell is connected to Side P and Side N of the DC voltage source through Diodes D_1 to D_6, energy is output from the DC voltage source only to the load.

As shown in Fig. 2, each output of pair Cells "INV_U and INV_X", "INV_V and INV_Y" and "INV_W and INV_Z" that are allocated between P and N of V_{DC} are connected respectively through Reactor L_{boost}. This reactor L_{boost} is used to charge Capacitor C_{DC} from the DC voltage source so that the boost effect can be secured for the capacitor voltage and energy can be exchanged between capacitors of each inverter cell.

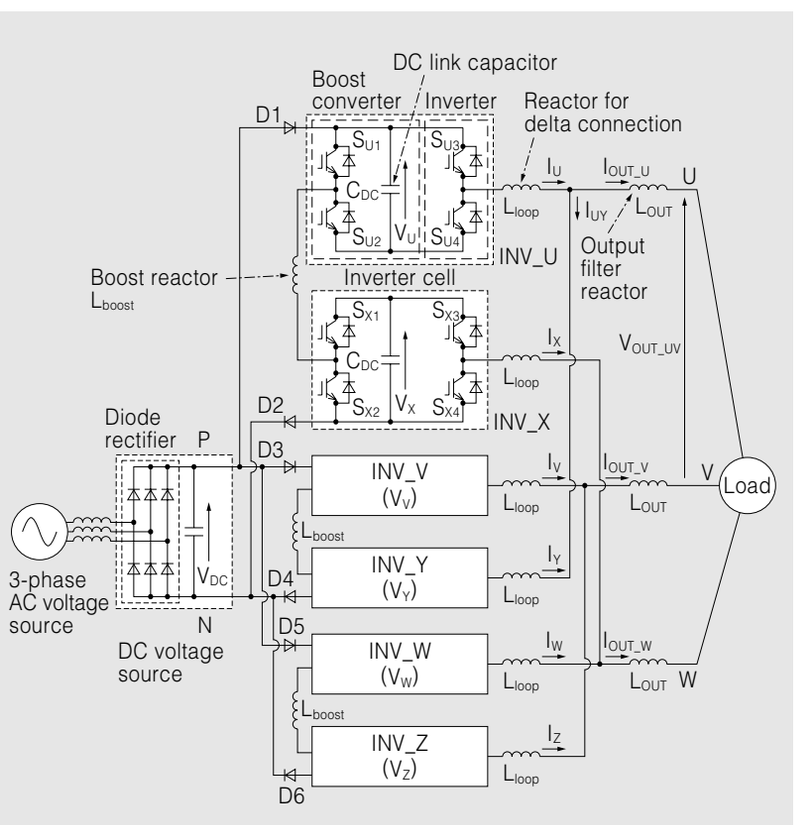

Fig. 2 Boost Type Multilevel Delta-Connected Cascade Inverter

The boost type multilevel delta-connection cascaded inverter is shown. In this circuit, it does not need DC voltage sources which are generated by the multiphase transformer and diode rectifiers for the respective inverter cells.

The output terminals of each inverter cell are connected in a delta shape with Reactor L_{loop} and are connected from their center point to the load through Reactor L_{out}. Reactor L_{out} functions as a filter to reduce

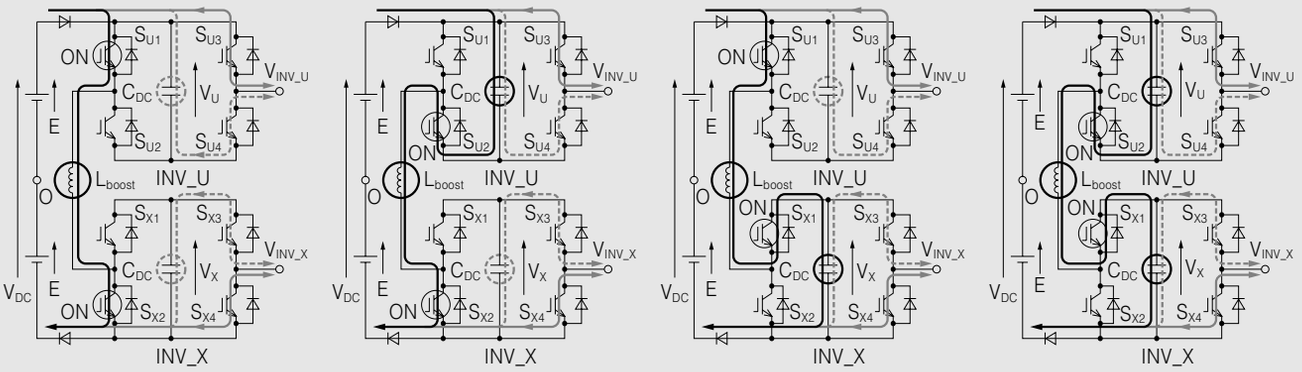

Fig. 3 Diagrams Explaining the Basic Principle of Operation
This figure shows the charging pattern where Capacitor C_{DC} of each inverter cell is charged from the DC voltage source and also the relationship in output terminal voltages.

output harmonics.

Compared with the two different connections of conventional cascade inverters shown in Fig. 1, the boost type multilevel delta-connection cascaded inverter does not need any multiphase transformer and is constructed of a DC voltage source and a diode rectifier. For the conventional cascade inverters shown in Fig. 1, a DC voltage is applied to the capacitor voltage for each cell, and stepped voltage is output in load. In contrast, the sine wave voltage with a few distortions is output in load because the condenser voltage of each cell is variable for this inverter.

3.2 Basic Principle of Operation

Fig. 3 shows the diagrams that explain the basic principles of operation. Explanations here are based on the inverter cells "INV_U and INV_X." As shown in the figure, there are four modes in which capacitor C_{DC} is charged for the inverter cells "INV_U and INV_X" from the DC voltage source. The voltage is output by the output terminals of the inverter cells while charging and discharging a capacitor C_{DC}.

Because energy stored in L_{boost} in Mode 1 is transferred to C_{DC} by modal transfer, the capacitor voltage can be boosted.

At the next stage, the DC voltage source V_{DC} is replaced with two voltage sources having Voltage "E" that are regarded as DC voltage sources for the respective cells. Based on the neutral point O, the output terminal voltages of the respective cells are defined as V_{INV_U} and V_{INV_X}. Voltage V_{INV_U} can produce a voltage output of "E" in a switching mode or Voltage "$E - V_U$" that is obtainable by subtracting E from the capacitor voltage V_U. Similarly, V_{INV_X} can produce a voltage output of "$-E$" or Voltage "$-E + V_X$" that is obtainable by adding $-E$ to the capacitor voltage V_X. Since V_U and V_X can be controlled to be variable by making a modal changeover of capacitor charging, the output terminal voltages of "$E - V_U$" and "$-E + V_X$" also become variable. Since each inverter cell can generate a variable voltage output, the line voltage

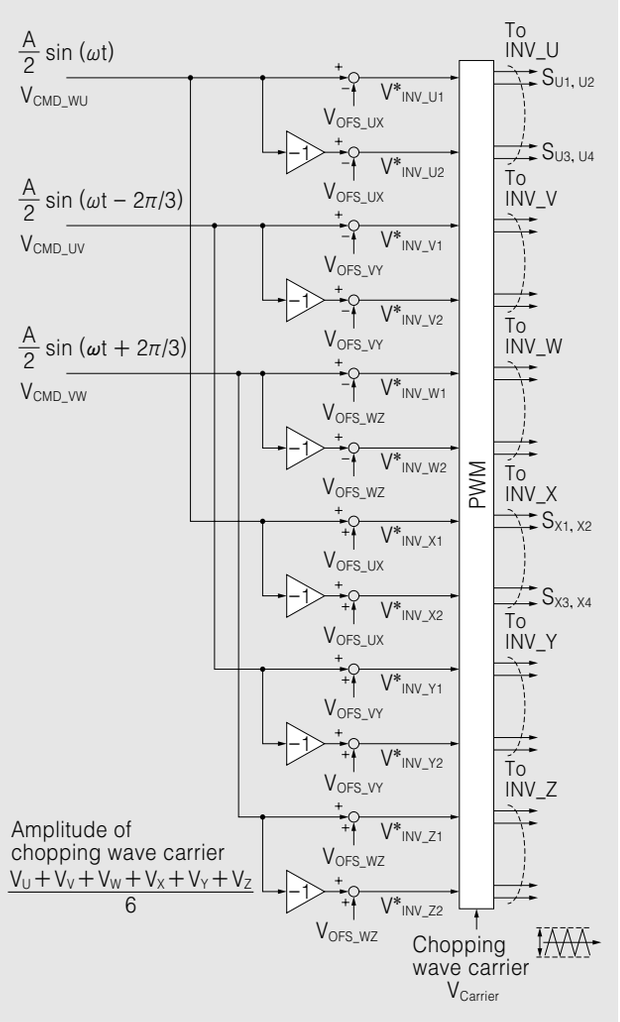

Fig. 4 Control Block Diagram
The control block diagram of the boost type multilevel delta-connection cascaded inverter is shown.

appearing between the output terminals of the two inverter cells is an output voltage with a low distortion factor. Similarly, since the output terminal voltages of inverter cells "INV_V and INV_Y" and also those of "INV_W and INV_Z" are variable, the line voltage can be a sinusoidal wave voltage with minimal distortion.

4. PWM Control and Offset Voltage Control

Fig. 4 shows the control block diagram. This inverter controls the line voltage of output. In order to control the two inverter cells "INV_U and INV_X" connected in series through Reactor L_{boost}, a voltage command value of V_{CMD_WU} is applied, that has half the amplitude of the line voltage between W and U. Similarly, other voltage command values of V_{CMD_UV} and also V_{CMD_VW} are applied to control the inverter cells "INV_V and INV_Y" and "INV_W and INV_Z." Command value voltages on boost converter side and inverter side of the respective inverter cells are inverted before they are applied. It is compensated with an offset voltage, and each command value voltage is applied to the PWM block. The compensated offset voltages of "V_{OFS_UX}," "V_{OFS_VY}," and "V_{OFS_WZ}" are set up so that they have the same absolute values and opposite signs in "INV_U and INV_X," "INV_V and INV_Y," and "INV_W and INV_Z." With the PWM block, the command value voltage "$V^*_{INV\_U1}$" is compared with "$V^*_{INV\_Z2}$" by carrier so that the gate signal output can be sent to each inverter cell. To control capacitor voltages so that all inverter cells are the same, the amplitude of the chopping wave carrier is set at the mean value of capacitor voltages of cells.

The effect of offset voltage compensation is explained below. Figs. 5 and 6 show the switching pattern where offset voltage compensation is performed and not performed, respectively. "$V^*_{INV\_U1}$," "$V^*_{INV\_U2}$," "$V^*_{INV\_X1}$," and "$V^*_{INV\_X2}$" in Figs. 5 and 6 show the command voltage values of "INV_U and INV_X" while "$V_{Carrier}$" denotes the chopping wave carrier. The right section of each figure shows the switching pattern in one period of the chopping wave carrier that is shown on the left side.

When offset voltage compensation is not performed, Mode 1, Mode 2, and Mode 3 of the switching pattern appears in a section shown in Fig.5 sequentially. In the section of Mode 1, energy is stored in Reactor L_{boost} and the capacitor voltage is boosted when a modal changeover to another mode is made. Therefore, if the period of Mode 1 is extended, the capacitor voltage is boosted excessively.

On the other hand, when offset voltage compensation is carried out, the command voltage value is changed as shown in Fig. 6. If comparison of switching modes is made in the same section as that shown in Fig. 5, the section of Mode 1 disappears and Mode 4 appears instead. In Mode 4, Capacitor C_{DC} of each inverter cell is charged up through L_{boost}. At that time, each capacitor voltage is maintained at "E." Accord-

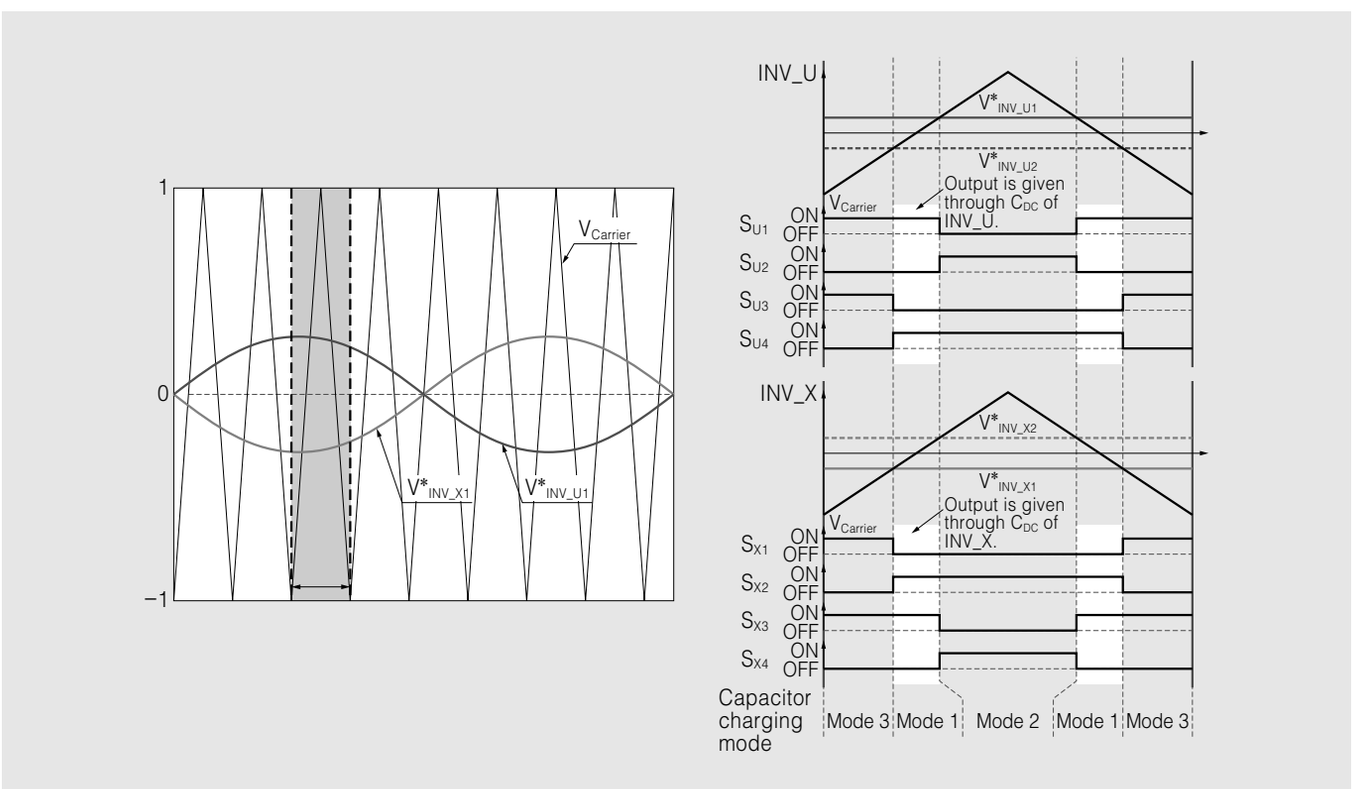

Fig. 5 Switching Pattern without Offset Voltage Compensation

The diagram at left shows the relationship between reference voltage of each inverter cell and carrier. The diagram at right shows the switching pattern of one carrier period shown in the left diagram.

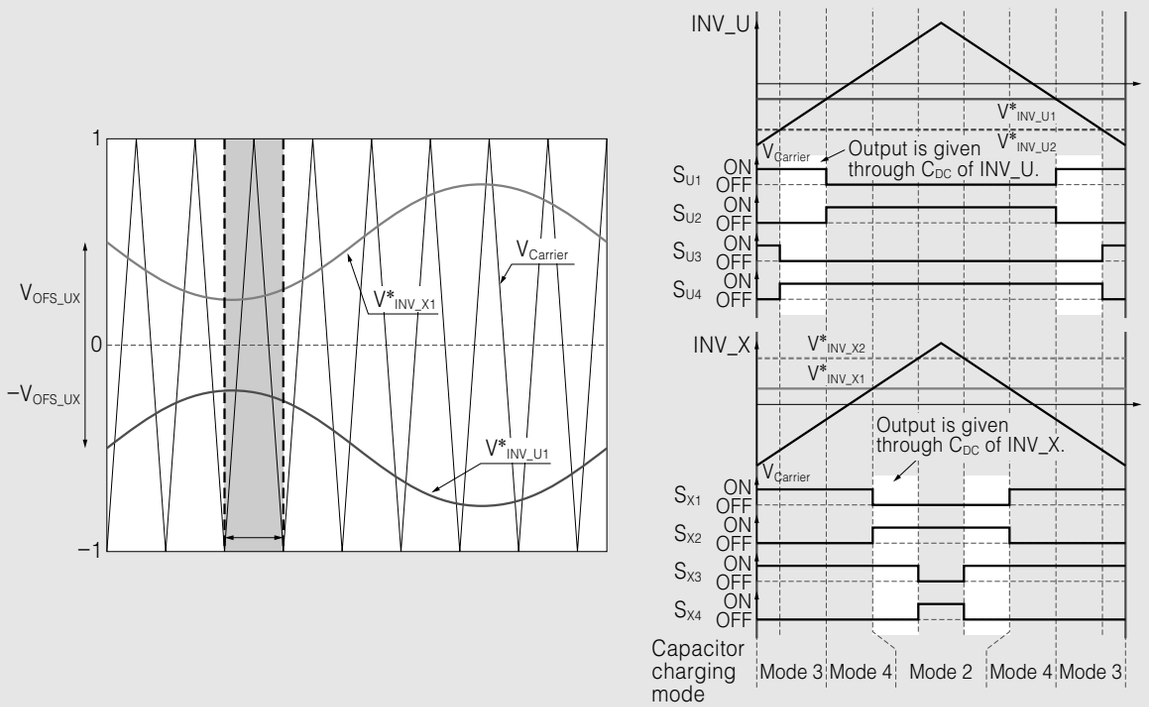

Fig. 6 Switching Pattern with Offset Voltage Compensation

The diagram at left shows the relationship between reference voltage of each inverter cell and carrier. The diagram at right shows the switching pattern of one carrier period shown in the left diagram.

ingly, it is possible to suppress excessive voltage boosting and obtain an arbitrary boosted voltage if the amount of offset voltage compensation is adequately adjusted.

As a result of offset voltage compensation, the charging and discharging pattern of capacitors in each cell is also changed. If no offset voltage compensation is made, the switching pattern becomes such that capacitor charge and discharge in the two inverter cells of "INV_U and INV_X" are performed with the same timing. In the case of offset voltage compensation, on the other hand, the switching pattern becomes such that capacitor charge and discharge are performed with a different timing. Therefore, offset voltage compensation yields a smaller voltage step in a line voltage of output. In addition, the resultant voltage waveforms involve lower distortion factors.

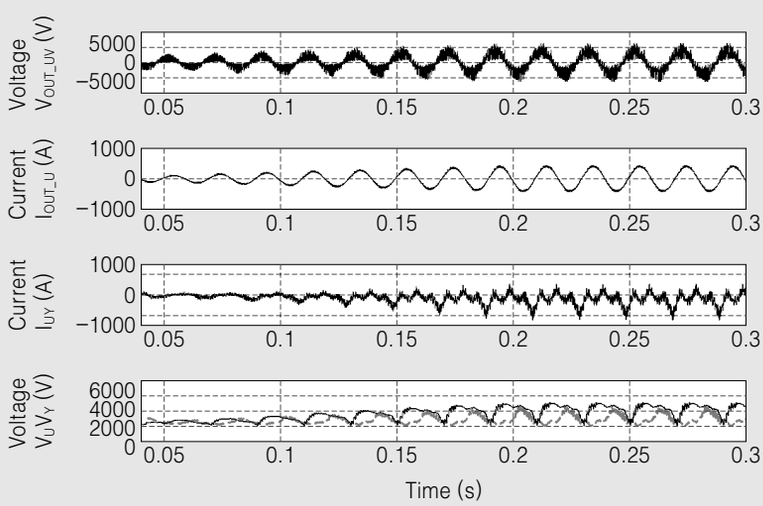

Fig. 7 Simulation Waveforms

From the top, the waveforms shown correspond to line output voltage V_{OUT_UV}, output current I_{OUT_U}, differential current I_{UY}, and DC capacitor voltages V_U and V_Y, respectively.

5. Simulation

Fig. 7 shows the result of simulation. Simulation conditions as shown in Table 1 were used for the simulation. The overall DC voltage is assumed to be 2000V and the load voltage is 3.3kV to examine the boost function. Fig. 7 shows the waveforms of simulation with a compensation of 0.25p.u., for the offset voltages of V_{OFS_UX}, V_{OFS_VY}, and V_{OFS_WZ}, respectively. From the top to the bottom in the graph, the waveforms correspond to line voltage of output V_{OUT_UV}, output current I_{OUT_U}, current flowing in delta connection I_{UY}, and capacitor voltages V_U and V_Y, respectively. The line voltage of output comes in a sinusoidal waveform containing minimal distortion. Each capacitor voltage was boosted

Table 1 Simulation Condition

Conditions of simulation for the proposed circuit are shown.

Input ratings	DC voltage	V_{DC}	2000V
Circuit parameter	DC link capacitor	C_{DC}	292μF
	Boost reactor	L_{boost}	0.8%※
	Reactor for delta connection	L_{loop}	1.6%※
	Output filter reactor	L_{out}	5.2%※
PWM	Carrier frequency	f_c	1kHz
Load ratings	Active power	1800kW	
	Reactive power	200kvar	
	Rated voltage	3.3kV	
	Output frequency	50Hz	

Note. "※ mark" is based on the load ratings.

as high as around 4000V and its pulsation was about 2000V. Given the above results, we could verify the boost function.

6. Postscript

This paper introduced a new circuit technology for the cascaded multilevel inverter that is operated by a single DC voltage source without using any multiphase transformers. This type of inverter offers the same performance characteristics as those of a conventional cascaded inverter. It also enables a boost function and results in low distortion of output voltage by changing the capacitor voltage as a variable voltage. At the same time, to make the output side into a delta connection, it requires many reactors.

Going forward, we will make research on the balance control method of capacitor voltage and study the application area which effectively uses the boost function of a cascade inverter.

《References》

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