Cu-SiO_2 Surface Activation by Ozone-Ethylene-Radical Process for Chip-to-Chip and Chip-to-Wafer Hybrid Bonding

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Abstract

We have attempted to replace the uncontrollable wet hydrophilization process with highly controllable dry process by using Ozone-Ethylene-Radical generation (OER). The atomically flat 5μm-square Cu-electrodes embedded in surrounding SiO_2 were treated with OER prior to hybrid-bonding, and the electrical resistance of Cu μ-joints were evaluated. Resistance value of 3-4 mΩ/μ-joint was achieved for OER treated dies, which is close to the resistance value for citric acid and N_2-plasma pretreated dies. We have also realized the electrical connectivity of 100,000 μ-joints.

1. Introduction

Hybrid bonding (HB) is one of the 3D-heterogenenous integration methods, where the dielectric and patterned metal surfaces are bonded with high alignment accuracy at room temperature followed by permanent bonding. HB allows one to realize sub-micron width interconnection with very high interconnect density at less than 1 μm pitch level[1].

By and large the chip-to-chip and chip-to-wafer HB involves the acid (citric acid (CA) $C_6H_8O_7$ or HCl or H_2SO_4 or HCOOH etc.) cleaning followed by O_2 or N_2 or Ar plasma activation to create an tangling bond/nanopores on the SiO_2 surface and finally the attachment of -OH moieties to the tangling bond through hydrophilization of SiO_2 surface[2]. Any kind of wet processes are uncontrollable when compared with the dry processes. There are two major concerns associated with the wet processes used in Cu-SiO_2 HB, and they are (1) uncontrollable wet processes invariably end up with the trapping of excessive cleaning acid material or the H_2O after the surface cleaning and hydrophilization; (2) the hydrophilization of SiO_2 surface after the plasma activation leads to a collateral damage on Cu surface. The exposure of Cu surface to O_2 plasma and H_2O molecule or hydroxyl (-OH) moiety leads to the formation of copper oxide (CuO_x) layer on the Cu electrodes. It is well known that Cu is highly prone to reacting with oxygen resulting in to the formation of cuprous oxide (Cu_2O) or cupric oxide (CuO)[3]. This CuO_x layer will act as a barrier for Cu diffusion between the electrodes resulting into an increase in contact resistance.

Therefore it is worth to find a suitable an alternative method for the surface activation of the dielectric material surface, which involves neither O_2 plasma nor H_2O molecule. Very recently, dry process called Ozone-Ethylene-Radical generation (OER) process was used for plasma activation cum deposition process for SiO_2 liner surface along the TSV sidewall, which was developed by the MEIDENSHA Corporation (Japan).

The merits of this OER process are (1) it does not involve any water , and hence there is no trapped water molecule at the bonded surface, and (2) since it directly produces -OH moiety by the chemical reaction between the pure O_3 and C_2H_4 gases in controlled low pressure environment, the process can be optimized to minimize the unreacted -OH moiety left at the bonded surface.

In the present work, we have attempted to evaluate the positive effect of OER process activation of SiO_2 surface with the conventional wet hydrophilization SiO_2 surface for HB.

2. Experimental

Our daisy-chain layout consists of 5 μm x 5 μm Cu electrode with the thickness value of 1.5 μm on both top and bottom dies which are embedded in SiO_2 matrix. TEG patterns were formed on 12" wafer level with the chip size of 6 mm and 7 mm squares respectively for top and bottom dies. After the Cu- chemical mechanical polishing (CMP), the dies were singulated by saw dicing for chip-to-chip and chip-to-wafer HB.

After forming the embedded Cu electrodes on 12" wafers by Cu-electroplating, wafer level Cu-CMP was performed to remove the overburden Cu and thus revealing the Cu-SiO_2 surface.

The hydroxyl radical ((OH)*) was formed *in-situ* by the controlled and sequential mixing of pure O_3 (200 sccm) and C2H4 (40 sccm) gases. The amount of formed (OH)* was monitored real-time using quartz crystal microbalance manufactured by NIHON DEMPA KOGYO Co., LTD., and time-invariant substantial amount of radical (e.g., (OH)*) generation was confirmed in a custom-made OER process chamber. The OER activation was carried out for 1 min. After the OER process, the top and bottom chips were flip-chip bonded at room temperature using 10 N applied pressure for 1 minute in air ambient. These bonded chips were loaded into the wafer bonder for permanent bonding under N2 atmosphere for 2 hours at 400 C with the applied pressure of 500-1000 N/chip.

3. Results and Discussion

It is inferred from the contact angle values that the shelf-life of (OH)* terminated SiO_2 surface does not deteriorate even after 30 hrs. of storage in N_2 ambient. While the air ambient stored (OH)* terminated SiO_2 surface stared losing the hydrophilic nature for the initial 5 hours, followed by a gradual deterioration with time.

After the flip-chip bonding followed by the permanent bonding, the bonded dies were checked for alignment accuracies using Infra-Red microscope. For both CA and OER treated dies, the alignment accuracy was 1-2 μm.

These X-sectional samples were observed FE-SEM, and the SEM image is shown in fig. 1. From the SEM image it can be inferred that a seem-free Cu-Cu bonding interface was obtained in the bonded dies formed from OER treated top and bottom dies.

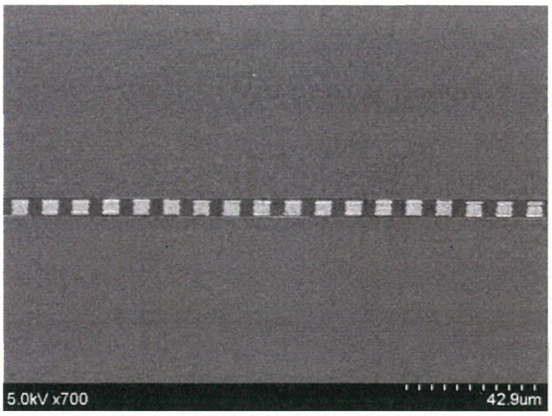

Fig. 1: Cross sectional SEM image obtained for 5 μm-size Cu-Cu μ-joints at 10 μm pitch values . SEM image did reveal an alignment accuracy of less than 100 nm between the top and bottom Cu electrode.

Finally, to confirm the integrity of the OER process in pretreatment of dies for the Cu-SiO_2 HB process, we have evaluated the electrical characteristics of 5 μm x 5 μm size Cu-Cu μ-joints at 10 μm pitch interval in the daisy chain configuration. Our TEG pattern consists of 100,000 electrodes and the wirings were made to measure the resistance for a single μ-joint to 100,000 μ-joints. Shown in Fig. 2 is the four-probe I-V characteristics of daisy chain segment containing 5,000 μ-joints. The measured resistance value is around 33~34 mΩ/μ-joint which includes the metal line resistance. Since the calculated metal line resistance which connects the Cu μ-joints in the daisy chain is around 30 mΩ/μ-joint, the measured

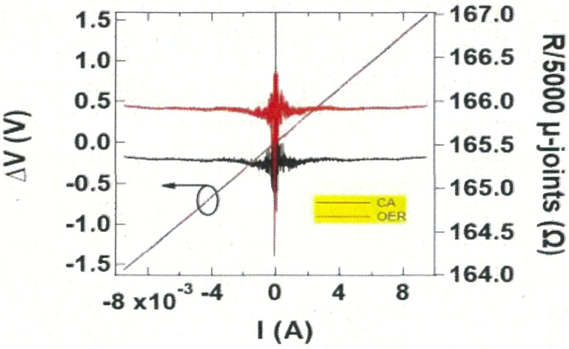

Fig. 2: I-V characteristics of single daisy-chain segment with 5000 Cu-Cu μ-joints at 10 μm pitch values.

resistance value of single Cu-Cu μ-joint is 3~4 mΩ which is slightly smaller than the theoretical resistance value 4.6 mΩ/μ-joint. For comparison we have also carried out chip-to-chip HB using CA pretreated chips. The resistance values of 100,000 μ-joints measured at every 5,000 μ-joints intervals for both CA and OER treated samples are almost similar.

4. Conclusions

We have proposed and demonstrated an alternative dry process method to the conventional two steps wet followed by plasma pretreatments for Cu-SiO_2 surface prior to chip-to-chip and chip-to-wafer HB process. A resistance value of 3-4 mΩ/μ–joint was achieved for both the CA pretreated and dies pretreated by OER process. This confirms that our proposed OER process for the pretreatment of dies is not only on par with any other conventional chip pretreatment methods for HB, but also free of acid and H_2O which causes reliability issue.

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